Course Number and Name

BEC702 - DIGITAL CMOS VLSI

Credits and Contact Hours

4 and 60

Course Coordinator's Name

Ms M.Jasmin

Text Books and References

1. Weste and Harris: CMOS VLSI DESIGN (Third edition) Pearson Education, 2005
2. Uyemura J.P: Introduction to VLSI circuits and systems, Wiley 2002.
3. D.A Pucknell & K.Eshraghian Basic VLSI Design, Third edition, PHI,2003
4. Wayne Wolf, Modern VLSI design, Pearson Education, 2003
5. M.J.S.Smith: Application specific integrated circuits, Pearson Education,1997
6. J.Bhasker: Verilog HDL primer, BS publication,2001
7. Ciletti Advanced Digital Design with the Verilog HDL, Prentice Hall of India, 2003
8. *https://en.wikipedia.org/wiki/Very-large-scale_integration*

Course Description

- To learn basic CMOS Circuits.
- To learn CMOS process technology.
- To learn techniques of chip design using programmable devices.
- To learn the concepts of designing adders and multipliers.

Prerequisites	Co-requisites
Principles of Digital Electronics	-

required, elective, or selected elective (as per Table 5-1)

Required

Course Outcomes (COs)

CO1 To learn about IC fabrication, MOS transistor action and its parameters.

CO2 Express the Layout of simple MOS circuit using Lambda based design rules.

CO3 About the design of various adders and multipliers in VLSI technology.

CO4 About the design styles of FPGA.

CO5 About testing of CMOS circuits.

CO6 To understand the concepts of modeling a digital system using Hardware Description Language

Student Outcomes (SOs) from Criterion 3 covered by this Course

COs/SOs	a	b	c	d	e	f	g	h	i	j	k
CO1	M							H	M		
CO2	M		H					M	H	H	
CO3	M		M	H						H	H

	CO4	M				H			M		H	
	CO5		H							H		
	CO6	H				H						H

List of Topics Covered

UNIT I INTRODUCTION TO MOS TRANSISTOR 12

MOS Fabrication, Enhancement mode and Depletion mode MOSFET, ,Threshold voltage derivation – body effect – Drain current Vs voltage derivation – channel length modulation – CMOS technologies, CMOS Fabrication: n-well – p-well – twin tub –DC transfer characteristics

UNIT II MOS CIRCUITS DESIGN PROCESS AND CMOS LOGIC GATES 12

MOS Layers, Stick Diagram, Layout Diagram, Propagation Delays, CMOS Static Logic Transmission Gate Logic, Tri-State Logic , Pass Transistor Logic , Dynamic CMOS Logic , Domino CMOS Logic,., Differential Cascade Voltage Switch (DCVS) Logic, Scaling of MOS Circuits.

UNIT III VLSI IMPLEMENTATION STRATEGIES 12

Introduction – Design of Adders: carry look ahead-carry select-carry save. Design of multipliers: Array – Braun array – Baugh-Wooley Array. Introduction to FPGA – Full custom and Semi custom design, Standard cell design and cell libraries, FPGA building block architectures.

UNIT IV CMOS TESTING 12

Need for testing- Testers, Text fixtures and test programs- Logic verification- Silicon debug principles- Manufacturing test – Design for testability – Boundary scan

UNIT V SPECIFICATION USING VERILOG HDL 12

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level, switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

Total: 60 Periods